

GP 2814
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Atty. Docket No.: 0819-0255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Hiroshige HIRANO et al.

Serial No.: 09/333,049

Filed: June 15, 1999

For: FERROELECTRIC MEMORY
DEVICE



Group Art Unit: 2814

Examiner: Hoai Pham

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on July 13, 2000

[Signature]

AMENDMENT TRANSMITTAL LETTER

Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is an Amendment for the above-identified patent application.

[X] No additional claim fee is required.

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AMENDED CLAIMS					
	NO. OF CLAIMS	HIGHEST NO. OF CLAIMS PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	ADDT'L FEE
Total Claims	10	MINUS 20 =	0	x \$18 =	0
Independent Claims	1	MINUS 3 =	0	x \$78 =	0
If Amendment adds multiple dependent claims, add \$260.00					0
Total Amendment Fee					0
If small entity status is claimed, subtract 50% of Total Amendment Fee					0
TOTAL ADDITIONAL FEE DUE FOR THIS AMENDMENT					N/A

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Application Serial No. 09/333,049
Attorney's Docket No. 0819-0255

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 19-2380(0116-214). This paper is submitted in duplicate.

Respectfully submitted,

NIXON PEABODY LLP

By: 

Eric J. Robinson
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EJR/BCO/ejb
Attorney Docket No.: 0819-0255

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AMENDMENT

Commissioner for Patents
Washington, D. C. 20231

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Sir:

In response to the Office Action mailed January 13, 2000, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 1 and 2 as follows:

- sub B*
1. (Amended) A ferroelectric memory device comprising:
a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;
a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;
- [Handwritten mark]*

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